REMARKS

Amendments

Claims 1, 5-7, 9-11, 16-20, 22-24, 31-33, 38-40, and 42-44 are amended herein.

Examiner Interview Summary

In a telephonic conversation between Examiner Horace Flournoy on May 4, 2007, and the below-signed attorney, Andrew C. Walseth, the Examiner and Applicant's Representative discussed the subject matter disclosed by the Present Application, the pending claims of the Present Application, and the Non-Final Office Action of February 8, 2007.

The Examiner and Applicant's Representative specifically discussed non-volatile memory commands to the driver or controller versus the low level write and erase accesses that make up the implementation of a given command and alter individual non-volatile memory cells, thus altering the permanent state of the associated non-volatile memory device(s). Applicant's Representative noted that the Present Application enabled determinate debugging, determinate power loss recovery testing and other memory driver/controller operations by tracking/stepping the individual low level write/erase accesses to memory device(s), instead of exhaustive empirical statistical testing of power loss recovery or stepping of individual system clock cycles. The Examiner and Applicant's Representative discussed various suggested amendments to the claims. The Examiner stated that the claims may be allowable over the cited references if amended to include an iterating test cycle, and clarifying that a write and erase access cycles are low level accesses that alter individual non-volatile memory cells and make up the implementation of a given command, but noted that further search may be necessary.

Applicant believes the foregoing interview summary accurately reflects the substance and scope of the interview and requests notification if the Examiner disagrees with the accuracy or completeness of the interview summary.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-2, 5-11, 13-33, 35-40 and 42-44 were rejected under 35 U.S.C. § 102(b) as being anticipated by Sekine (U.S. Patent No. 5,896,398) with Microsoft Computer Dictionary (MSCD), 5th edition offered as extrinsic evidence. Applicant respectfully traverses this rejection and submits that claims 1-2, 5-11, 13-33, 35-40 and 42-44 are allowable for at least the following reasons.

Applicant respectfully notes that non-volatile memory commands and low level write and erase accesses are defined in the Specification, at least, at Paragraphs [0007], [0014]-[0015], [0023], and [0032]-[0039].

In particular, Applicant notes that Paragraph [0007] states, in part, "[h]owever, as data write operations, block erasures, and other internal Flash management operations that store or change data or the operating state of the Flash memory device are generally not single step operations, the Flash memory can be left in an incomplete state by a power loss event. For example, a make directory command requires 43 separate write/erase operations by the driver of a specific Flash memory device to complete. Because of these issues the driver software contains 'power loss recovery' routines that sequence the Flash memory device through a power loss recovery cycle to check for such uncompleted operations upon power up, and, if possible, finish or correct them."

Applicant also respectfully notes that prior art testing of drivers and non-volatile memory devices, for correct operation, system debugging and testing of power loss recovery cycles and drivers routines in prior art Flash memory devices and systems is described in Paragraphs [0007]-[0008]. In particular, power loss recovery cycles are noted as having generally involved randomized power loss testing by removing power from the system at a random point during a selected write, erase, or Flash memory management operation and then restoring power to test the power loss recovery cycle and associated driver routines.

Applicant further notes that stepping of non-volatile memory write and erase accesses during access of Flash commands to test are detailed in the Specification, at least, at Paragraphs [0011], and [0032]-[0034].

In particular, Applicant notes that Paragraph [0032] states, "[i]n embodiments of the present invention, the driver counts the number of write or erase operations for executing a selected Flash operation and then halts/interrupts execution at a selected write or erase operation. At this point the state of the processor and/or contents of the memory and registers can be inspected if desired. If the system is then brought back up again this tests the power loss recovery for the selected halt point in the Flash command and allows a known and definite testing coverage of the Flash memory device and driver for a particular case. This quantifies the power loss case for that particular software environment (and if desired, physical environment). In one embodiment, the counting of write or erase operations and/or halting/interrupting execution is done by a function incorporated into the low level driver. In one embodiment only

write or only erase operations are counted. In another operation both write and erase operations are counted."

In the rejection the Examiner specifically stated that Sekine disclosed "'[a] *method of operating a non-volatile memory* **[Sekine discloses in column 1, line 13, 'A flash memory is a non-volatile IC memory ...']** *device driver* **[The MSCD defines 'device driver' on page 155 as 'a software component that permits a computer system to communicate with a device...' Sekine teaches a device driver, in column 7, lines 26-30.]** *comprising: counting a number of write and/or erase* **[Sekine discloses in column 1, lines 31-35, 'In this patent specification, the present invention is explained in detail mainly with respect to the write function, but it can be similarly applied to the erase function of the flash memory as well.']** *access cycles to a nonvolatile memory without regard to a failure of the write and/or erase access cycle;* **[disclosed e.g. in column 1, lines 54-63. Sekine teaches a memory for fail analysis (FIG. 4, element 18) which is separate from (without regard to) the Test processor of FIG. 4, element 11.]** *and halting access to the non-volatile memory at a selected count."* **[column 7, lines 19-21, '...when the writing test is repeated until the predetermined maximum number of times, the process terminates and proceeds to the next test.' Also see column 7, lines 35-40.]"**

Applicant respectfully continues to disagree and maintains that Sekine teaches a Flash memory test system that tests Flash memory devices by writing data to the memory device being tested and reading it back to find defective memory elements in the arrays. In doing so, Sekine reads back the test data written into the memory device, unlike the pending claims of the Present Application; and writes this test data not a predetermined number of times, as maintained by the Examiner, but only until the test data written into the memory device reads back correctly. After successfully reading back the correct test data, the Flash memory test system of Sekine, moves on to the next test or memory address to be tested. The Flash memory test system of Sekine only fails the address location if a maximum number of write attempts to the address without a correct read back of the test data has been exceeded; if a successful write occurs, the Flash memory test system of Sekine never reaches the maximum number of write attempts while testing a given location. Applicant thus maintains that this is not counting a number of low level write and/or erase access cycles of a non-volatile memory command without regards to a success or failure of the low level write and/or erase access cycles to a non-volatile memory and halting execution at a selected count, but writing and reading test data to an address location until a successful data write occurs, or failure occurs.

Sekine states at Column 7, Lines 6-25, "The fail analysis memory 18 gives a write enable inhibit signal /WE to the wave formatter 14 for the address of the MUT 5 whose stored data agrees with the expected data, thereby prohibiting the system from repeating the write operation for the same address any further. *The write operation is repeated for the remaining addresses whose data does not agree with the expected data until the stored data agrees with the expected data or until the predetermined maximum numbers of write operation have been performed.* During this repeated write and read process, in case where all of the addresses attain PASS (match) results, the process terminates by sending an MF (match flag) signal from the fail analysis memory 18 to the pattern generator 13. Alternatively, when the writing test is repeated until the predetermined maximum number of times, the process terminates and proceeds to the next test. The fail analysis memory 18 stores the results of the data writing test to be used in the fail analysis stage of the MUT 5." {Emphasis Added}

Applicant therefore continues to respectfully maintains that Sekine teaches a Flash memory test system that tests Flash memory devices after they have been manufactured by writing data to the Flash memory device(s) being tested and reading it back to find defective memory elements in the arrays and not a method of operating a non-volatile memory device driver comprising counting a number of low level write and/or erase access cycles of a non-volatile memory command to a non-volatile memory and halting execution at a selected count. Specifically, Applicant respectfully maintains that Sekine, Column 4, Lines 42-45 and Column 7, Lines 19-21 does not teach or disclose counting a number of low level write and/or erase access cycles to a non-volatile memory of an executing non-volatile memory command without reading a state of any memory cell of the non-volatile memory device altered by the access cycles and halting access to the non-volatile memory at a selected count of low level write and/or erase access cycles, but counting the number of write operations required for a successful data write or data write failure (when a maximum number of repetitions is reached) at a specified address of the flash memory. After which the flash memory test system does not halt, but moves on to the next test pattern or address. As such, Applicant respectfully maintains that Sekine does not teach or disclose counting to a selected count value of low level write and/or erase access cycles without reading a state of any memory cell of the memory altered by the low level access cycles or without regard to the success or failure of the access operations, but counting the number of write and read accesses that occur until write failure is determined, if a successful write occurs the test at that location is complete. Applicant also maintains that Sekine does not teach or disclose halting access to the non-volatile memory at a selected count value of low level write

and/or erase access cycles and executing a power loss recover routine and then changing the selected halt count and re-executing the non-volatile memory command, but moving to next test, test pattern or memory address upon the occurrence of a successful write or the occurrence of the number of attempts that determine a write failure. (*See*, Sekine, Figure 3; Column 7, Lines 15-39; Column 7, Line 58 to Column 8, Line 29; and Column 4, Lines 41-45.)

Further, Applicant has carefully reviewed the reference Sekine and has found no mention of the Flash memory test system removing power from the Flash memory under test or executing a power loss recovery operation on the Flash memory device under test contrary to the Examiner's assertions. As such the Applicant continues to respectfully maintain that Sekine does not disclose or teach removing power from the Flash memory under test or executing a power loss recovery operation on the Flash memory device under test.

Applicant therefore, as outlined above, respectfully submits that Sekine fails to teach or disclose a method of counting the number of low level write and/or erase accesses to a non-volatile memory device of an executing non-volatile memory command without reading a state of any memory cell of the non-volatile memory device altered by the write and/or erase accesses and halting when a selected number of low level write and/or erase accesses is reached. As such, Sekine fails to teach or disclose all elements of Applicant's claims.

Applicant's claim 1, as amended, recites "[a] method of operating a non-volatile memory device driver comprising: counting a number of low level write and/or erase access cycles of a non-volatile memory command to a non-volatile memory without regard to a failure of the low level write and/or erase access cycle, wherein each low level write and/or erase access cycle modifies the state of at least one non-volatile memory cell of the non-volatile memory; halting access to the non-volatile memory at a selected count of low level write and/or erase access cycles; changing the selected count; re-executing the non-volatile memory command; counting the number of low level write and/or erase access cycles; and halting access to the non-volatile memory at the changed count of low level write and/or erase access cycles." As detailed above, Applicant submits that Sekine fails to teach or disclose such a method of operating a non-volatile memory device driver that counts the number of low level write and/or erase access cycles of a non-volatile memory command to a non-volatile memory without regard to a failure of the write and/or erase access cycles and halts access to the non-volatile memory at a selected count. As such, Sekine fails to teach or disclose all elements of independent claim 1.

Applicant's claim 11, as amended, recites "[a] method of operating a system comprising: counting a number of low level write and/or erase access operations of a command to a Flash

memory device coupled to a host without regard to a failure of the write and/or erase access operations, wherein each low level write and/or erase access operation modifies the state of at least one non-volatile memory cell of the Flash memory; stopping access execution to the Flash memory at a selected number of access operations; changing the selected number of access operations; re-executing the command; counting the number of low level write and/or erase access operations; and stopping access execution to the Flash memory at the changed selected number of access operations." As detailed above, Applicant submits that Sekine fails to teach or disclose such a method of operating a system to count the number of low level write and/or erase access operations of a Flash memory command to a Flash memory device coupled to a host without regard to a failure of the low level write and/or erase access operations, and stop access execution to the Flash memory at a selected number of access operations. As such, Sekine fails to teach or disclose all elements of independent claim 11.

Applicant's claim 20, as amended, recites "[a] method of testing a Flash memory comprising: counting a number of access operations to a Flash memory for a Flash command without regard to a failure of altering a state of any memory cell of the Flash memory altered by the access operations, wherein the access operations are low level write and/or erase access operations to the Flash memory to execute the Flash command and where each low level write and/or erase access operation modifies the state of at least one non-volatile memory cell of the Flash memory; interrupting execution of the Flash command at a selected halt count of access operations, halting access to the Flash memory; executing a power loss recovery cycle to test power loss recovery at the selected halt count; changing the selected halt count; re-executing the Flash command; counting the number of access operations; and interrupting execution of the Flash command at the changed halt count." As detailed above, Applicant submits that Sekine fails to teach or disclose such a method of testing a Flash memory. As such, Sekine fails to teach or disclose all elements of independent claim 20.

Applicant's claim 31, as amended, recites "[a] method of profiling a Flash command comprising: counting a number of low level access operations to a Flash memory during execution of a Flash command without regard to a success or failure of the access operations to create an access operation profile for the Flash command, wherein the low level access operations alter the state of at least one non-volatile memory cell of the Flash memory; and comparing the access operation profile of two or more Flash commands." As detailed above, Applicant submits that Sekine fails to teach or disclose such a method of profiling a Flash command. As such, Sekine fails to teach or disclose all elements of independent claim 31.

Applicant's claim 33, as amended, recites "[a] system comprising: at least one Flash memory device; and a host coupled to the at least one Flash memory device, wherein the host is adapted to: count a number of low level write and/or erase access operations to the at least one Flash memory device during execution of a Flash command without regard to a success or failure of the write and/or erase access operations, wherein each low level write and/or erase access operation modifies the state of at least one non-volatile memory cell of the Flash memory, halt execution of the Flash command, stopping access to the Flash memory device at a selected count of low level write and/or erase access operations, execute a power loss recovery routine on the at least one Flash memory device, change the selected count of low level write and/or erase access operations, and re-execute the Flash command." As detailed above, Applicant submits that Sekine fails to teach or disclose such a system wherein the host is adapted to count a number of low level write and/or erase access operations to the at least one Flash memory device during a Flash command without regard to a success or failure of the low level write and/or erase access operations and halt execution of the Flash command, stopping access to the Flash memory device at a selected count of low level access operations, changing the halt count and re-executing the Flash command. As such, Sekine fails to teach or disclose all elements of independent claim 33.

Applicant's claim 40, as amended, recites "[a] machine-usable medium, the machine-usable medium containing a software routine for causing a processor to execute a method, wherein the method comprises: counting a number of low level write and/or erase access cycles to a Flash memory during execution of a Flash command without reading any non-volatile memory cells written or erased by the write and/or erase access cycles , wherein each low level write and/or erase access cycle modifies the state of at least one non-volatile memory cell of the Flash memory; halting execution at a selected count of low level write and/or erase access cycles, halting access to the Flash memory; changing the selected halt count of low level write and/or erase access cycles; re-executing the Flash command; counting a number of low level write and/or erase access cycles; and halting execution at the changed count of low level write and/or erase access cycles." As detailed above, Applicant submits that Sekine fails to teach or disclose such a machine-usable medium having a method that counts a number of low level write and/or erase access cycles to a Flash memory without reading any non-volatile memory cells written or erased by the low level write and/or erase access cycles and halts access to the Flash memory at a selected count low level write and/or erase access cycles. As such, Sekine fails to teach or disclose all elements of independent claim 40.

Applicant's claim 43, as amended, recites "[a] system comprising: at least one Flash memory device; and a host coupled to the at least one Flash memory device, wherein the host comprises a means for counting a number of low level write and/or erase access cycles to the at least one Flash memory device during execution of a Flash command without regard to a success or failure of the write and/or erase access cycles and where each low level write and/or erase access cycle modifies the state of at least one non-volatile memory cell of the Flash memory device; wherein the host comprises a means for halting execution of the Flash command on the at least one Flash memory device in response to the count of the access cycle counting means, stopping access to the Flash memory device at a selected halt count; wherein the host comprises a means for changing the selected halt count of the access cycle counting means; wherein the host comprises a means for re-executing the Flash command; wherein the host comprises a means for counting the number of access operations with the access cycle counting means; and wherein the host comprises a means for interrupting execution of the Flash command at the changed halt count." As detailed above, Applicant submits that Sekine fails to teach or disclose such a system. As such, Sekine fails to teach or disclose all elements of independent claim 43.

Applicant respectfully contends that claims 1, 11, 20, 31, 33, 40 and 43 as pending has been shown to be patentably distinct from the cited reference. As claims 2, 5-10, 13-19, 21-30, 32, 35-39, 42, and 44 depend from and further define claims 1, 11, 20, 31, 33, 40 and 43, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(b) and allowance of claims 1-2, 5-11, 13-33, 35-40 and 42-44.

Claim Rejections Under 35 U.S.C. § 103

Claims 35 and 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sekine (U.S. Patent No. 5,896,398) in view of Kim (U.S. Published Application No. 2003/0075609 A1). Applicant respectfully traverses this rejection and submits that claims 35 and 36 are allowable for the following reasons.

Applicant continues to respectfully maintain, as stated above, that Sekine fails to teach or suggest all elements of claim 33, from which claims 35 and 36 depend from. As such, Applicant respectfully maintains that Sekine also fails to teach or suggest all elements of claim 33. In addition, Applicant continues to maintain that Kim discloses a memory card having an improved transmission speed and that memory cards include SMC, MMC and Memory Stick interface designs and can include NAND and NOR flash memory, but does not teach or disclose a method

of counting the number of low level write and/or erase accesses of an executing Flash command to a Flash memory device without regard to a success or failure of the low level write and/or erase access operations and halting when a selected number of low level write and/or erase accesses are reached. Sekine also does not teach or suggest changing the halt count and re-executing the Flash command. Applicant further respectfully maintains that Kim fails to teach or disclose a Flash memory device having one of a PCMCIA-ATA, a Compact Flash (CF), a USB Flash, and a Secure Digital Memory Card compatible interface. *See*, Kim, Abstract and Paragraphs [0005], [0019], and [0023]. Applicant therefore respectfully submits that combining the elements of Sekine with Kim fails to teach or suggest all elements of independent claim 33, and thus also fails to teach or suggest all elements of dependent claims 35 and 36, either alone or in combination.

Applicant respectfully contends that claim 33 as pending has been shown to be patentably distinct from the cited references, either alone or in combination. As claims 35 and 36 depend from and further defines claim 33 they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 35 and 36.

CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. Please charge any further fees deemed necessary or credit any overpayment to Deposit Account No. 501373.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

Date: 5/8/07

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